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Rapid joule heating of metal films used to crystallize silicon films

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Abstract. We analyzed the rapid heating properties of 50-nm-thick silicon films via 250-nm-thick SiO_2 intermediate layers by heat diffusion from joule heating induced by electrical current flow in chromium strips. Numerical heat-flow simulation resulted in that the silicon films were heated to the melting point by a joule-heating intensity above 1 MW/cm^2. A marked increase in electrical conductance associated with silicon melting was experimentally detected. Taper-shaped chromium strips detected the temperature gradient in the lateral direction caused by the spatial distribution of the joule-heating intensity. Crystallization occurred according to the temperature gradient. A 2–4-μm lateral crystalline grain growth was demonstrated for the silicon films.

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Rapid annealing is attractive for the formation of polycrystalline silicon (poly-Si) films at low processing temperatures and the application of poly-Si to fabrication of electrical devices such as thin film transistors (TFTs) [1–10]. Laser crystallization has been widely used for the rapid formation of polycrystalline silicon films. Poly-Si TFTs with good performances have been reported. For laser crystallization, optical equipment is required in order to deliver the laser beam to samples and to control the distribution of laser beam intensity. We have proposed a simple crystallization method using electrical-current-induced joule heating of silicon [11]. Silicon films have been rapidly heated and crystallized through heat diffusion from thin metal films heated by electrical-current-induced joule heating.

In this paper, we report the analysis of the heating properties of silicon with chromium metal thin films as a heating source. The rapid increase of temperature at the silicon layer to the melting point is analyzed using numerical heat-flow analysis. A transient conductance measurement is also presented in order to observe silicon melting. We also report the crystallization of silicon films in the lateral direction using taper-shaped chromium strips.

1 Experimental

Undoped amorphous silicon films with a thickness of 50 nm were formed by low-pressure chemical vapor deposition (CVD) methods on quartz glass substrates. 250-nm-thick SiO_2 films were formed on the silicon films by sputtering. 100-nm-thick chromium films were subsequently formed on the SiO_2 films. Chromium strips with a width of 80 μm were defined by etching. Aluminum electrodes with a gap of 500 μm were also formed on the chromium strips in order to apply electrical voltages to the chromium strips with a low contact resistance. The resistance of chromium strip was 150 Ω. Pulsed voltages with a duration of 3 μs were applied to the samples, as shown in Fig. 1a. The electrical current was measured as a voltage V_1 at the 1.5-Ω-load resistance R_1, connected between the sample and ground using a digital oscilloscope. The high electrical current flowing through the chromium strips caused a high joule-heating intensity per unit area $P(t)$ given as:

$$P(t) = \frac{\left(V_0 - V_1\left(1 + \frac{R_s}{R_1}\right)\right) V_1}{R_1 S}, \quad (1)$$

where V_0 is the applied voltage, R_s is the series resistance, 5 Ω, of the circuit and S is the area of the chromium strips. The joule heat generated in the chromium films diffuses into the underlying layer and the silicon films are heated by heat flow through the intermediate SiO_2 layer.

In order to experimentally investigate silicon melting by the present heating method, transient conductance measurements were carried out. Phosphorus-doped (1×10^{20} cm^{-3}), 50-nm-thick silicon strips with a width of 10 μm were defined on quartz substrates. Aluminum electrodes with a gap of 20 μm were formed on the silicon strips. 250-nm-thick SiO_2 films were subsequently formed as the intermediate layer by sputtering. 100-nm-thick chromium strips a width of 80 μm

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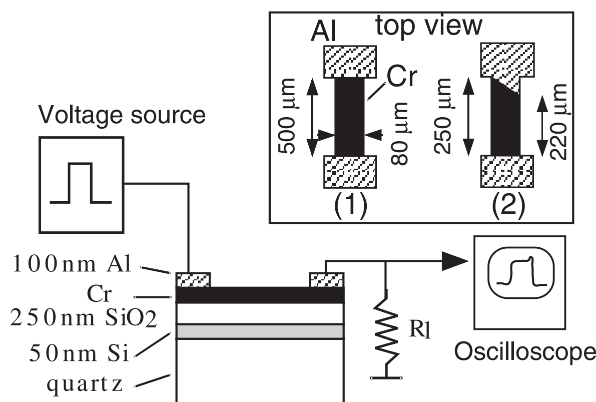


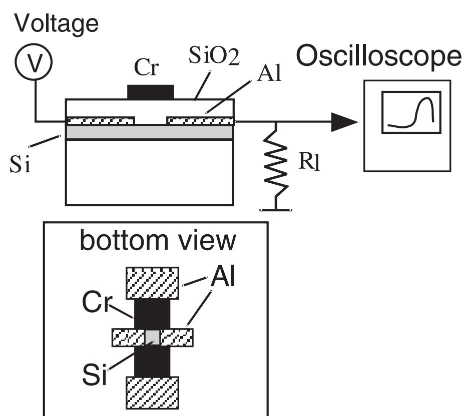


Fig. 1a,b. Schematic of the apparatus of the presented electrical-current-induced joule-heating method and the cross section of the layered structure of the samples. **a** A 3-µs-pulsed voltage was applied to the chromium strip formed on 250-nm-thick SiO_2/50-nm-thick silicon layers. *Inset* presents a simple strip with a length of 500 µm, a width of 80 µm and a thickness of 100 nm (1) and a taper-shaped strip with a length of 250 µm at the wide edge, 220 µm at the narrow edge and with a width of 50 µm and a thickness of 60 nm (2). **b** The apparatus for transient conductance measurement. Silicon strips with a width of 10 µm and a length of 20 µm were placed below chromium strips having a length of 500 µm, a width of 80 µm and a thickness of 100 nm. A voltage of 1 V was applied to the silicon strips for measuring the change in the electrical conductance of silicon during and after the joule heating

and a length of 500 µm were formed on the SiO_2 films above the silicon strips, as shown by the inset in Fig. 1b. The electrical current flow in silicon strips was measured by applying a voltage of 1 V across the aluminum gaps during the presence of joule heating [12].

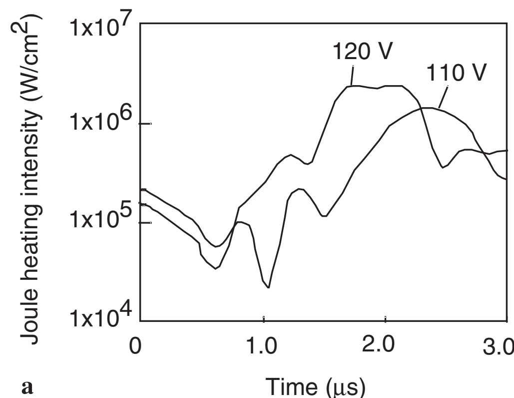
In order to investigate crystallization in the lateral direction, taper-shaped chromium strips with a width of 50 µm were also fabricated by the formation of a slant edge in the aluminum gap electrodes at one side, as shown by inset (2) in Fig. 1a. The chromium strip therefore had a length changing from 250 µm at the long edge to 220 µm at the narrow edge. The chromium strips had a thickness of 60 nm and a resistance of 320 Ω.

We used Raman scattering measurements in order to investigate the crystalline states of the silicon films with a spectrum resolution of 4 cm^{-1}, using a 514.5-nm Ar-ion laser. We used transmission electron microscopy (TEM) to observe the distribution of the crystalline grains. We also observed the distribution of crystalline grains using a wet-etching method [13]. During the dipping of the silicon films in a solution containing 2 g of CrO_3 powder and 2 cm^3 of 50% HF, diluted with 200 cm^3 of pure water, for 6 min, amorphous and disordered silicon regions were etched out and crystalline regions with large grains remained.

2 Results and discussion

Figure 2 shows the changes in the intensity of the electrical-current-induced joule heating generated in the chromium strips at the applied voltages of 110 and 120 V for 3 µs. The joule heating intensity decreased with time in the initial stage because the resistivity of chromium increased due to joule self heating. Afterwards, a rapid increase in the joule heating intensity was observed from about 1 µs after the voltage was applied, as shown in Fig. 2. The joule heating intensity then increased above 1×10^6 W/cm^2. This increase in the joule heating resulted from a decrease in the resistivity, probably associated with initiation of the melting of the chromium strips due to joule self heating to the melting point (2485 K) [14].

Temperature changes in the chromium and silicon layers caused by time-dependent joule heating were estimated using a numerical analysis program. The program was constructed



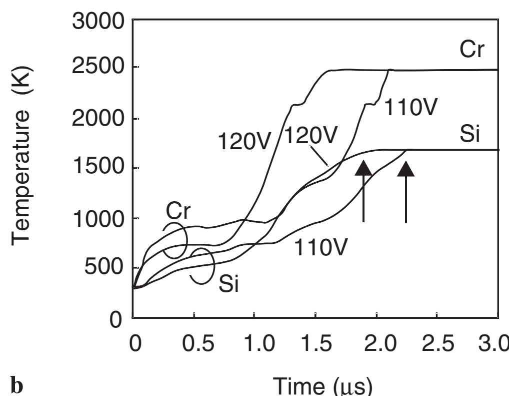


Fig. 2a,b. Electrical current and joule-heating intensity generated in the chromium strips as a function of time with voltages of 110 V and 120 V applied to the chromium strips (**a**) and calculated changes in temperature of the chromium layers and the silicon layers using the joule-heating intensity (**b**)

two-dimensionally with a system of heat flow equations derived from a heat-balance condition at each of a set of points along the depth and width directions, in order to analyze the temperature distribution for a multi-layered structure with different materials [15]. For the point of $(i,\ j)$, the equation is expressed by:

$$\frac{T_{i,j}^{n+1}-T_{i,j}^{n}}{\Delta t}=\frac{Q_{i,j}^{n}}{c_{i,j}\varrho_{i,j}}+\frac{1}{\Delta^2}\left(\sum_{l=-1}^{+1}D_{i+l,j}^{i,j}\left(T_{i+l,j}^{n}-T_{i,j}^{n}\right)+\sum_{m=-1}^{+1}D_{i,j+m}^{i,j}\left(T_{i,j+m}^{n}-T_{i,j}^{n}\right)\right), \qquad (2)$$

where $T_{i,j}^{n}$ is the temperature at time t_n of the point of $(i,\ j)$, $D_{i+l,\ j+m}^{i,j}$ is the average thermal diffusivity constant between points of $(i,\ j)$ and $(i+l,\ j)$, $c_{i,j}$ is the specific heat, $\varrho_{i,j}$ is the density of weight and $Q_{i,j}$ is the heating intensity per unit volume at point of $(i,\ j)$. The temperatures of the silicon thin films were determined by the heat balance between the heat supply from the joule heating intensity and heat dissipation into glass substrates. $D_{i+l,j+m}^{i,j}$, $c_{i,j}$ and $\varrho_{i,j}$ and the latent heat energies are given for chromium, silicon and SiO_2 in Table 1 [14–16]. Temperature changes in the chromium and silicon layers were calculated for joule heating in the 110 V and 120 V cases. We assumed that chromium and silicon were melted at their melting points, respectively, and that the temperature was kept at the melting points until the latent heat was given to the layers. We also assumed that the upper limit of the temperature of the chromium was the evaporation temperature.

Figure 2b shows the changes in the temperature of the top chromium layers and the underlying silicon layers, calculated using the joule-heating intensity for the 110 and 120 V applied voltages shown in Fig. 2a. The chromium layers were rapidly heated by the high intensity of the joule heating. The temperature of the chromium layers reached the melting point in 1.9 μs and 1.3 μs, for 110 V and 120 V, respectively. The chromium was further heated to the evaporation temperature in 2.1 μs and 1.7 μs for the 110 V and 120 V cases, respectively. The silicon layers were rapidly heated by heat diffusion from the top chromium layers via the intermediate SiO_2 layers. The temperature of the silicon layers reached the melting point in 2.3 μs and 1.9 μs for 110 V and 120 V, respectively. The heat flow simulation suggested that the silicon films could be melted by joule heating of the order of $10^6\ \mathrm{W/cm^2}$ generated in the overlying chromium layers. Melting of the silicon, followed by solidification to crystalline states, was expected.

In order to demonstrate experimentally the melting of the silicon layers, the change in electrical conductance of phosphorus-doped silicon was measured using the apparatus shown in Fig. 1b. Figure 3 shows the change of the electrical conductance measured during the joule heating at 120 V applied voltage. At the initial stage of the joule heating, the electrical current was very low, below the detection limit, because of the high resistance of the silicon strip. Marked increase in the electrical conductance was observed at 2.2 μs. The electrical conductance increased to 5.4 mS/sq during the joule heating. The result shows that the silicon films were melted by the rapid heat diffusion from the chromium strips. After joule heating, the electrical conductance decreased because of the solidification process. There was a residual conductance of 1.1 mS/sq at 5 μs resulting from the activation of phosphorus atoms and carrier generation associated with the crystallization of silicon.

We investigated the possibility of crystalline growth in the lateral direction. Taper-shaped chromium strips (see Fig. 1a) were used to cause a temperature gradient in the lateral direction in the silicon layers. The electrical resistance was high and the electrical current was low on the wide-length side of the chromium strip. Therefore, the joule-heating intensity was low. However, high joule heating could be generated on

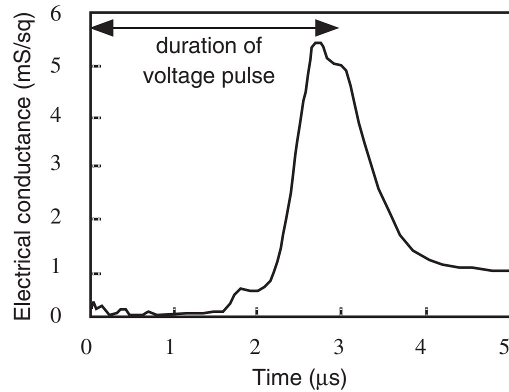


Fig. 3. Change in the electrical conductance of the phosphorus-doped ($1\times10^{20}\ \mathrm{cm^{-3}}$) silicon strips during and after joule heating at 120 V

Table 1. Thermal constants of the materials used for the heat-flow calculation

	Cr	Si	SiO_2
Density [g/cm^3]	7.2	2.33	2.27
Thermal diffusion coefficient [cm^2/s]	0.202	$1.861-4.2\times10^{-2}T+4.0\times10^{-6}T^2$ $-1.0\times10^{-9}T^3$	$2.5\times10^{-3}+7.0\times10^{-6}T$ (500 K > T > 300 K) 0.514 (T > 500 K)
Specific heat [J/gK]	0.46	$0.497+9.0\times10^{-4}T-5.0\times10^{-7}T^2$ $+9.0\times10^{-7}T^3$	$0.483+2.4\times10^{-3}T-2.0\times10^{-6}T^2$ $+4.0\times10^{-10}T^3$
Melting point [K]	2163	1685	–
Boiling point [K]	2485	–	–
Latent heat for fusion [J/g]	258	1810	–
Latent heat for vaparization [J/g]	6168	–	–

the narrow-length side because of the low resistance. Consequently, a spatial distribution of the joule-heating intensity in the width direction can be formed. We calculated the temperature change of the silicon layers in the lateral direction using the numerical heat-flow equation (1) when 120 V was applied to the chromium strips for 3 μs. The geometry of the taper-shaped strip gave a spatial distribution to the joule-heating intensity. The density of joule-heating intensity at a point x in the width direction in the chromium strips, $P(x, t)$, is given as

$$P(x, t) = \frac{\left(L_{\mathrm{w}}^2 - L_{\mathrm{n}}^2\right) W^2}{2\left(\ln L_{\mathrm{w}} - \ln L_{\mathrm{n}}\right)} \frac{P(t)}{\left((W-x)L_{\mathrm{w}} + xL_{\mathrm{n}}\right)^2}, \tag{3}$$

where W is the width of the strip of 50 μm, L_{w} is the widest length of the strip of 250 μm, L_{n} is the narrowest length of the strip of 220 μm and $P(t)$ is the joule heating intensity per unit area at t given by (1), which was experimentally determined.

Figure 4 shows the temperature distribution in the silicon layers in the width direction from the point just below the wide-length edge of the chromium strip to the point below the narrow-length edge at different times. In the initial stage of the joule heating, the temperature of the silicon film increased with time at every point. There was a temperature gradient in the silicon layer in the lateral direction. The temperature was high below the narrow-length chromium region because of the high-intensity joule heating. The silicon region below the narrow-length edge of the chromium strip was first heated to the melting point in 1.5 μs. The whole silicon region was heated to the melting point in 3 μs. After the termination of joule heating, the cooling process proceeded. The temperature decreased from the melting point in 3.5 μs at the region below the wide-length edge of the chromium strip to below the narrow-length edge of the chromium strip in 5.0 μs. The cooling rate at the liquid/solid interface was 1.8×10^8 K/s in 3.5 μs. It decreased to 1.2×10^8 K/s in 5.0 μs because of a reduction in temperature gradient in the depth direction associated with heat diffusion into the deeper region. The heat flow calculation suggested the possibility of melt regrowth of the silicon layer in the lateral direction; The solidification initiated from the region below the wide-length edge of the chromium strip. The liquid/solid interface proceeded towards the region below the narrow-length edge of the chromium strip according to the cooling process.

The silicon films treated with the tapered-shaped chromium strips were observed with an optical microscope after removing the chromium and aluminum layers. The color of the silicon films was changed from that of the initial amorphous silicon in the regions below the chromium, as shown in Fig. 5a. The color change indicated the crystallization of the silicon layers. Stokes–Raman scattering spectra were also measured. Some regions below the wide-length edge of the chromium strip shown in Fig. 5a had a broad peak around 460 cm^{-1}, associated with an amorphous bonding network, as shown in Fig. 5b. A very sharp crystalline transverse optical (TO) phonon peak was observed on the edge of the crystallized region as shown at (b) in Fig. 5a. The spectral line shape of the TO phonon peak was almost symmetrical, centering around 517 cm^{-1}, as shown in Fig. 5b. There was almost no broad peak on the low wavenumber side associated with the amorphous and nano-crystalline TO phonon. This indicated the formation of a crystalline region with little disordered bonding. In contrast, the interior region crystallized below the narrow-length of the chromium strip had a TO phonon band with a small broad peak on the low wavenumber side as well as sharp crystalline TO phonon peak. Formation of very small crystalline grains or disordered regions in the region was suggested, although the joule-heating intensity was high on the narrow-length side of the chromium strip.

The TEM observation was carried out after removing the chromium and aluminum layers, and the SiO_2 intermediate layers and etching the glass substrate by the ion

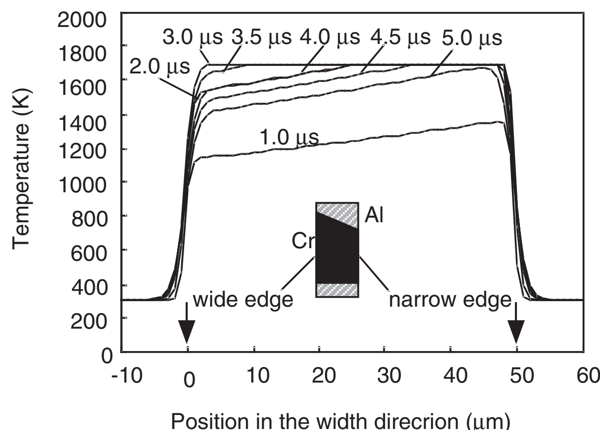


Fig. 4. Calculated temperature change of the silicon layer in the width direction for the taper-shaped chromium strips with a length of 250 μm at the wide edge and of 220 μm at the narrow edge and with 120 V applied

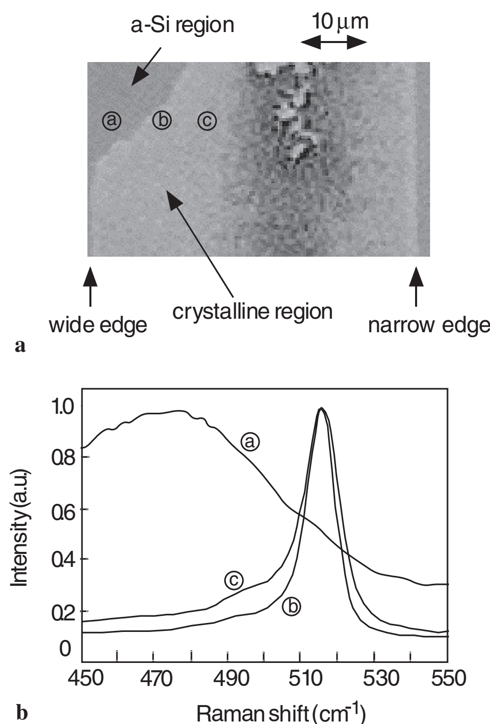


Fig. 5a,b. Photograph of optical microscope used for the silicon layers treated at 120 V with the taper-shaped chromium strips (**a**) and Stokes–Raman scattering spectra for different points (a)–(c) indicated in **a** (**b**). The spectra were normalized by their peak intensities

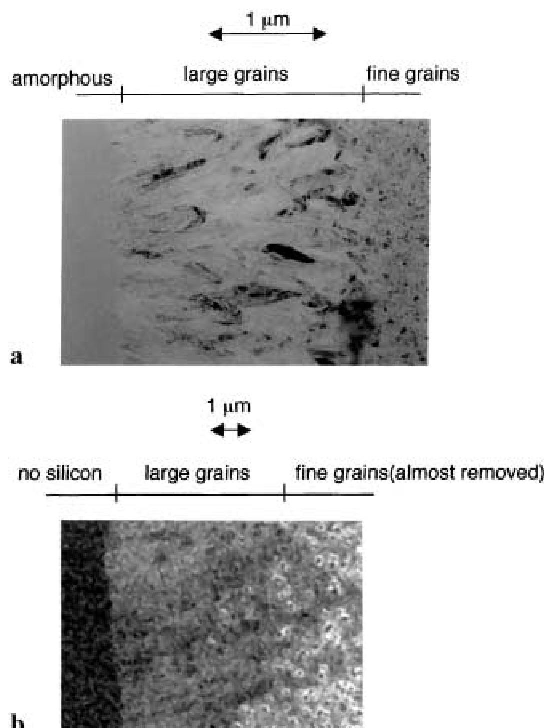


Fig. 6a,b. Photograph of the bright field image of the TEM plane view for the silicon layer crystallized at 120 V with taper-shaped chromium strips (**a**) and a photograph by SEM after dipping the samples in the solution of CrO_3 powders and HF diluted with pure water (**b**)

milling method from the rear surface. Figure 6a shows a photograph of the bright field image of the TEM plane view for silicon films crystallized by the present method with the taper-shaped chromium strip. At the edge of the crystallized region, which had a sharp TO phonon peak in the Raman scattering spectra, TEM observation revealed the formation of crystalline grains with a size of about 2 μm. The formation of 2-μm-long crystalline grains is interpreted by the fact that crystallization occurred laterally according to the temperature gradient formed in the width direction. The interior crystalline region had fine crystalline grains, with sizes ranging between 50 and 100 nm. We also observed crystalline regions for many samples using the wet etching method, in order to investigate the possibility of the formation of large crystalline grains. Figure 6b shows a photograph taken by SEM of the edge of the crystallized region. The treatment with a solution of CrO_3 powders and HF diluted with pure water removed the amorphous region and almost removed crystalline regions with small grains. Crystalline regions with large grains remained. The SEM photograph of Fig. 6b shows the formation of the largest crystalline grains, 4-μm-long in our present investigation. Observations using TEM and SEM indicate the possibility of the formation of large crystalline grains using the present crystallization method with an appropriate temperature distribution.

3 Summary

The rapid heating properties of joule heating, induced by electrical current flow in chromium strips, were analyzed in order to crystallize 50-nm-thick silicon films formed adjacent to 250-nm-thick SiO_2 films. A pulsed voltage at 120 V for 3 μs caused high-intensity joule heating above 1 MW/cm^2. Numerical heat-flow simulation indicated that the chromium strips were heated to evaporation temperature during the joule heating, and that the underlying silicon layers were heated to their melting point by heat diffusion from the chromium strips. The melting of silicon was experimentally determined by the measurement of the rapid increase in the electrical conductance of the silicon layers associated with the high conductivity of liquid silicon. Taper-shaped chromium strips with a length of 250 μm at the wide edge and of 220 μm at the narrow edge were applied to investigate the possibility of the crystallization of the silicon in the lateral direction. A two-dimensional-heat-flow calculation demonstrated that the spatial distribution of the joule-heating intensity induced a temperature gradient in the width direction. Raman scattering, TEM and SEM measurements revealed that joule heating with taper-shaped chromium strips at 120 V applied voltage for 3 μs formed crystallized regions with 2–4-μm-long grains and with little disordered bonding in the 50-nm-thick silicon films.

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