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Rapid crystallization of silicon films using Joule heating of metal films

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Abstract. 50-nm thick amorphous silicon films formed on glass substrates were crystallized by rapid Joule heating induced by an electrical current flowing in 100-nm-thick Cr strips formed adjacently to 200-nm-thick SiO_2 intermediate layers. 3-μs-pulsed voltages were applied to the Cr strips. Melting of the Cr strips caused a high Joule heating intensity of about 1×10^6 W/cm^2. Raman scattering measurements revealed complete crystallization of the silicon films at a Joule heating energy of 1.9 J/cm^2 via the SiO_2 intermediate layer. Transmission electron microscopy measurements confirmed a crystalline grain size of 50–100 nm. 1-μm-long crystalline grain growth was also observed just beneath the edge of the Cr strips. The electrical conductivity increased from 10^{-5} S/cm to 0.3 S/cm for 7×10^{17}-cm^{-3}-phosphorus-doped silicon films because of activation of the phosphorus atoms because of crystallization. The numerical analysis showed a density of localized defect states at the mid gap of 8.0×10^{17} cm^{-3}. Oxygen plasma treatment at 250 °C and 100 W for 5 min reduced the density of the defect states to 2.7×10^{17} cm^{-3}.

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Polycrystalline silicon films have been applied to many devices, such as thin-film transistors (TFTs) and solar cells [1–6]. Formation of poly crystalline silicon films at low cost has been demanded in recent years for the fabrication of large-area devices. Many technologies have been reported for formation of polycrystalline silicon films at low processing temperatures, such as pulsed-laser crystallization, plasma-enhanced chemical vapor deposition, catalytic chemical vapor deposition and metal-induced crystallization [1–10]. We have also developed a crystallization method using electrical-current-induced Joule heating of silicon [11–13]. When electrical current flows in silicon films, the silicon films are self-heated by Joule heating. Long melting for 100 μs and large crystalline grains (∼ 15 μm) have been demonstrated. In this paper we report another simple Joule heating method using metal thin films as heating sources in order to rapidly crystallize silicon films. Rapid Joule heating at an intensity of about 1.0 MW/cm^2 is demonstrated by allowing current to flow in chromium (Cr) metal strips. Crystallization of silicon films and activation of phosphorus atoms doped in the silicon films are reported. Through analyses of the electronic properties of the silicon films, the grain boundary properties are discussed. We also discuss the possibility of applying the present Joule heating method to device fabrication.

1 Experimental

Undoped 50-nm-thick amorphous silicon films were formed by low-pressure CVD methods on quartz-glass substrates. Some silicon films were doped with phosphorus atoms at 7×10^{17} cm^{-3} using the ion implantation method. 200-nm-thick SiO_2 films were formed on the silicon film by sputtering. 100-nm-thick Cr films were subsequently formed on the SiO_2 films. Cr strips with a length of 250 μm and a width of 50 μm were defined by etching. Al electrodes were also formed at the edge regions of the Cr strips to apply electrical voltages to the Cr strips with a low contact resistance. 3-μs-pulsed voltages were applied to the samples, as shown in Fig. 1. The electrical current was measured using the voltage V_1 across the 2.5-Ω load resistance R_1 connected between the sample and ground, using a digital oscilloscope. A high electrical current flowing in, the Cr strips causes a high Joule heating intensity per unit area W(t) given as $(V_0 - V_1 \times (1 + R_s/R_1)) \times V_1 \times (R_1 \times S)^{-1}$, where V_0 is the applied voltage, which was also detected with another digital oscilloscope, R_s is the series resistance of the circuit, and S is the area of the Cr strips. The Joule heat generated at the Cr films diffuses in the underlying layer and the silicon films are heated by heat flow through the intermediate SiO_2 layer.

We used Raman scattering measurements in order to investigate the crystalline states of the silicon films with a spectrum resolution of 4 cm^{-1}. A 514.5-nm Ar-ion laser was introduced to the silicon films from the rear side of the samples through quartz-glass substrates. We also used a transmission

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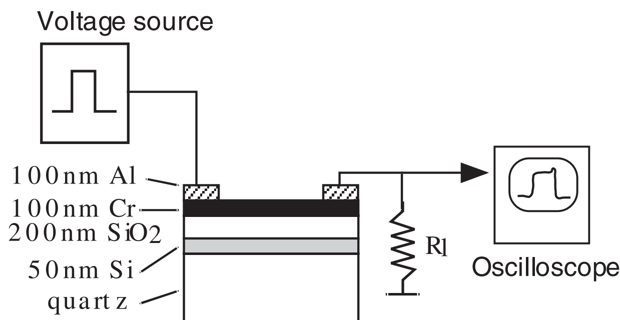

Fig. 1. Schematic apparatus of the present electrical-current-induced Joule heating method and the cross-section of the layered structure of the samples. 3-μs-pulsed voltages were applied to the 100-nm-thick Cr strip with a length of 250 μm and a width of 50 μm, which was formed on 200-nm-thick SiO_2/50-nm-thick silicon layers

electron microscope (TEM) to observe the distribution of the crystalline grains. The electrical conductivity was measured for phosphorus-doped silicon films in order to investigate the activation behavior of the phosphorus dopant atoms associated with the present heat treatment. For the measurements, the Cr strip and SiO_2 films were etched out using liquid solutions. Al gap electrodes were formed on the silicon films. A 13.56-MHz radio-frequency (RF) oxygen-plasma treatment was conducted at 250 °C at 100 W for 5 min to reduce the number of defect states in the silicon films [14].

2 Results and discussion

Figure 2 shows changes in the electrical current flowing in the Cr strips and the intensity of the electrical-current-induced Joule heating at applied voltages of 60, 70, 80 and 90 V. The electrical current decreased with time from the initial voltage application because the resistivity of Cr increased due to the electrical-current-induced Joule self-heating. Afterwards, an increase in the electrical current was observed at the time indicated by the arrows in Fig. 2. The point of increase in the electrical current occurred earlier for higher voltage applications. The maximum value of the electrical current also increased as the applied voltage increased, as shown in Fig. 2. This increase in the electrical current probably results from melting of Cr strips due to the Joule heating. The Cr strips were rapidly heated to a high temperature and then they were probably melted. It is natural that melting initiates earlier for higher Joule heating intensities with higher voltage applications. Assuming complete melting of the Cr layer in the case of 90-V application, the resistivity of the molten Cr layers was estimated at $8.0 \times 10^{-6}\,\Omega\,\text{cm} \pm 2 \times 10^{-6}\,\Omega\,\text{cm}$. From the experimental results of the electrical current, the Joule-heating intensity per unit area was estimated, as shown in Fig. 2. A Joule-heating intensity higher than $1 \times 10^5\,\text{W}\,\text{cm}^{-2}$ was observed for every applied voltage. It increased as the voltage increased. A Joule-heating intensity above $1 \times 10^6\,\text{W}\,\text{cm}^{-2}$ was achieved when the Cr strip was melted in the case of the 90-V application. Figure 3 shows the total Joule-heating energy density obtained by integration of the Joule-heating intensity during the pulse duration as a function of the voltage applied to the Cr films. The Joule-heating energy density was lower than 0.3 J/cm^2 for the 40- and 50-V applications. It markedly increased, from 0.75

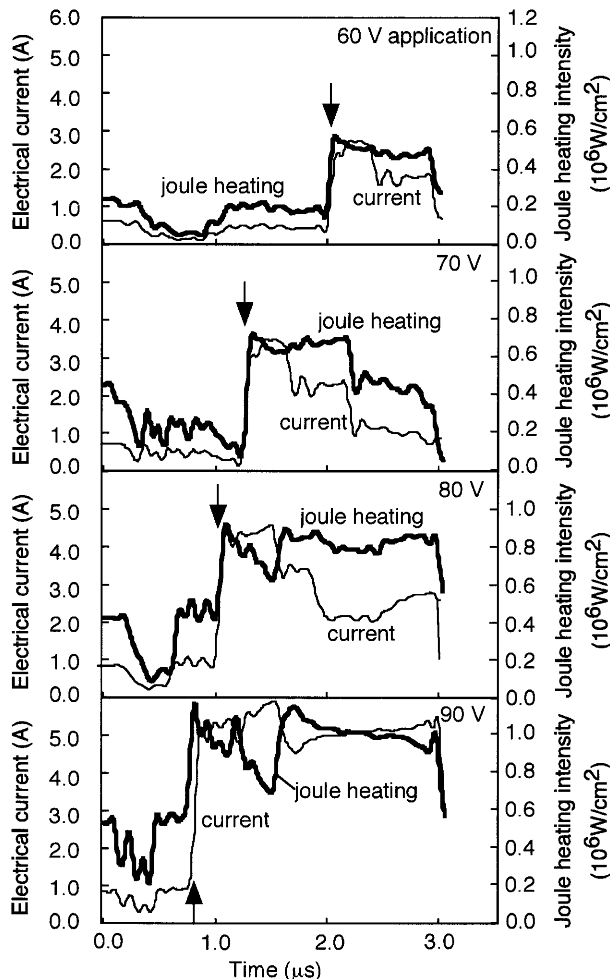

Fig. 2. Electrical current and Joule heating intensity generated at the Cr strips as functions time with different voltages applied to the Cr strips

to 2.45 J/cm^2 as the voltage increased from 60 to 90 V. High Joule-heating energy density results from the low resistivity of Cr metal due to Joule-heating-induced melting.

We estimated the temperature change of silicon caused by the time-dependent Joule-heating shown in Fig. 2 using

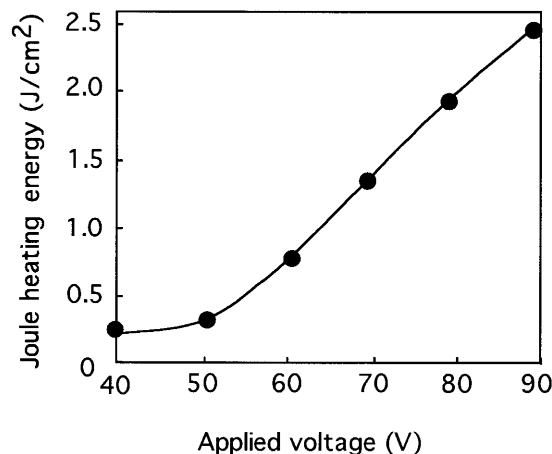

Fig. 3. Total Joule heating energy density obtained by integration of the Joule heating intensity during the pulse duration as a function of the voltage applied to the Cr strips

a numerical analysis program. The program was constructed with a system of heat flow equations derived from a heat-balance condition for each set of points along the depth, in order to analyze the temperature distribution for a multiple-layered structure with different materials. For the ith point, the equation used is [15, 16]

$$\frac{T_i^{n+1} - T_i^n}{\Delta t} = \frac{Q_i^n}{c_i \varrho_i} + \sum_{m=-1}^{+1} D_{i+m}^i (T_{i+m}^n - T_i^n) , \tag{1}$$

where T_i^n is the temperature at time t_n of the ith point, D_{i+m}^i is the thermal diffusivity constant between points i and $i+m$, c_i is the specific heat at point i, ϱ_i is the weight density at point i, and Q_i is the heating intensity per unit volume at point i and at time t_n. The temperatures of the silicon thin films were determined using the heat balance between the heat supply from the Joule heating intensity generated at the Cr top layer, as shown in Fig. 2, and heat dissipation into the glass substrates. We assumed that silicon melted at 1685 K for every heating case and the temperature was kept at the melting point until the latent heat energy (1810 J/g) was delivered to the silicon layer. Figure 4 shows the temperature change for silicon films 200 nm distant from the Cr strips during the electrical-current-induced Joule heating of the Cr strips. The calculation indicated that a voltage application above 70 V heated the silicon to melting point. The melt duration increased from 0.8 to 1.5 μs as the voltage increased from 70 V to 90 V. Although we do not know the precise thermal properties of the amorphous silicon which we used in the present experiments, the heat flow calculation suggests that the silicon films can be rapidly heated to a high temperature, reaching melting point, and that there is the possibility of a rapid melt followed by crystallization of silicon films.

Visual observation with an optical microscope from the rear side of the samples confirmed that the present heating at an application of 80 V caused a uniform change in the color of the undoped silicon films in the area underlying the Cr strips. However, the edge regions of the Cr strips connecting to the Al electrodes were broken after the Joule heating with voltages above 70 V. Figure 5 shows Stokes Raman scattering spectra for the initial amorphous silicon films and silicon films treated with the electrical-current-induced Joule heating, with different voltages applied to Cr films. The spectrum of as-deposited a-Si films showed a broad peak around 460 cm^{-1}. In the 70-V-voltage application case, the Raman spectra had a similar spectrum line shape to that of the as-deposited films. There was no crystalline *TO* phonon peak. The silicon film was still in the amorphous state. On the other hand, a sharp peak of crystalline *TO* phonon appeared in the spectrum for the sample heated at the 80-V application. The broad amorphous peak was markedly reduced. The Joule heating with a 80-V application provided a Joule-heating energy density of 1.9 J/cm^2. The Raman spectrum indicated that the heating energy density was high enough to change the present silicon films to a crystalline state via the 200-nm-thick SiO_2 intermediate layers. Joule heating with a 90-V application further increased the intensity of the crystalline *TO* phonon peak and reduced the intensity of the amorphous *TO* phonon band. The peak wavenumber of the crystalline *TO* phonon peak in the case of the 80-V application was 512 cm^{-1}, which was lower than that of the single crystalline form at 520.1 cm^{-1}. The low peak wavenumber means that the crystalline silicon films had a high tensile stress of 1.3×10^9 Pa [17] between the glass substrates and the SiO_2/Cr overlying layers. The full-width at half-maximum (FWHM) of the Raman band was 9 cm^{-1}, which was broader than that of the single crystalline, 2.8 cm^{-1}. We guess that the high tensile stress caused the damping of the lattice vibration and broadened the bandwidth [18].

Figure 6 shows a photograph of the bright-field image of the TEM-plane view for silicon films crystallized using the present method at 80 V. The silicon region underlying the Cr strips was completely crystallized. Fine crystalline grains with a size ranging between 50 and 100 nm were formed close to each other. On the other hand, the formation of 1-μm-sized crystalline grains was observed at the region underlying the edge of the Cr strips. The large crystalline grains were probably formed laterally according to a temperature distribution in the lateral direction associated with heat dissipation from the edge of the Cr strips during Joule heating. This TEM result indicates the possibility of forming large crystalline grains with an appropriate temperature distribution for the present crystallization method.

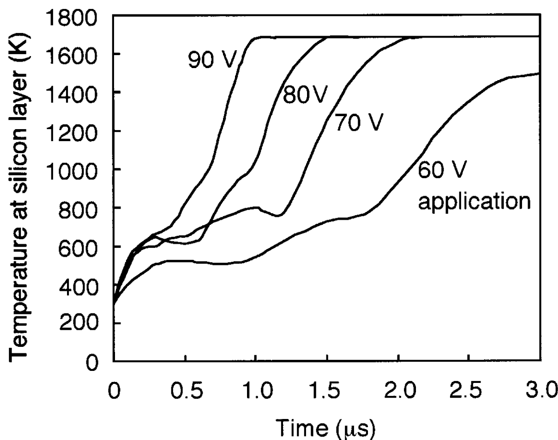

Fig. 4. Temperature change at the 50-nm-thick silicon films from initiation of the 3-μs-pulsed voltage application, estimated by numerical heat flow analysis assuming a 1685-K melting point of silicon

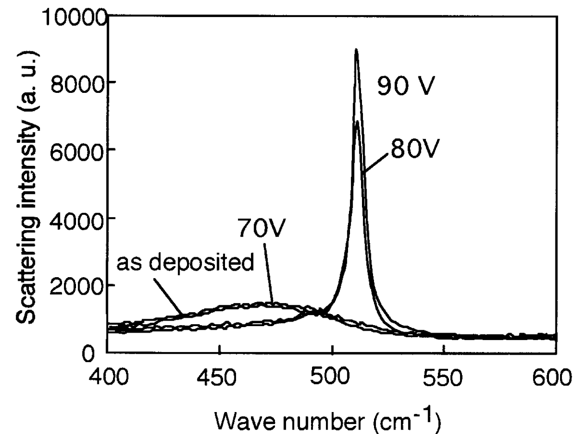

Fig. 5. Stokes Raman scattering spectra for initial amorphous silicon films and silicon films treated with the electrical-current-induced Joule heating with different voltages applied to Cr films

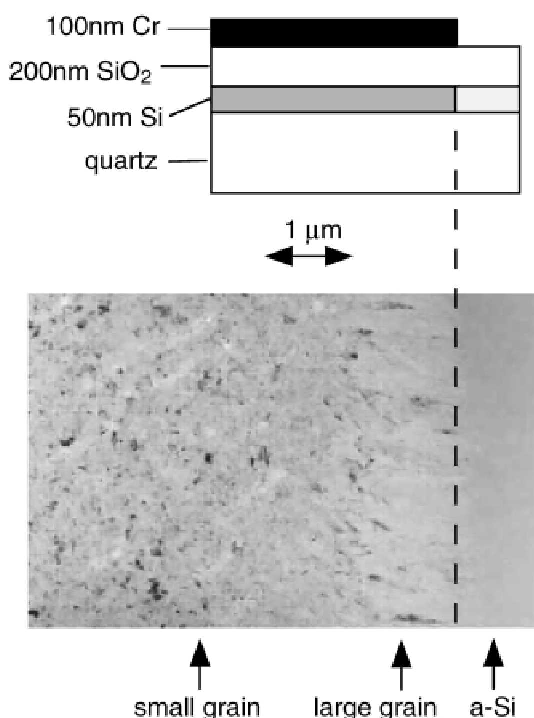

Fig. 6. Photograph of the bright-field image of the TEM-plane view for the 50-nm-thick silicon films crystallized by the present method at 80 V. The schematic cross-sections of the samples are also illustrated to identify the positions of the TEM observations

Figure 7 shows the electrical conductivity as a function of the applied voltage for the phosphorus-doped silicon films. The electrical conductivity was very low, 10^{-7}–10^{-6} S/cm for Joule heating with a voltage application between 50 and 60 V. On the other hand, it increased to 2×10^{-2} S/cm as the voltage increased from 65 to 75 V. The color of the silicon films also changed with 65-V heating. The increase in the electrical conductivity caused by the electrical-current-induced Joule heating means that the phosphorus atoms were activated and the electron carriers were generated by the heating. The increase in the electrical conductivity occurred at a Joule-heating energy density of 1.2 J/cm^2 with a 65-V application. That energy density was lower than that for the crystallization of undoped silicon films (1.9 J/cm^2). Our interpretation ist that ion implantation of the phosphorus atoms increases the number of disordered states in the silicon bonding network and reduces the melting threshold of the silicon films so that the doped silicon is crystallized and the dopant atoms are activated at the low heating energy density.

Moreover, the oxygen-plasma treatment further increased the electrical conductivity to 0.3 S/cm. The increase in the electrical conductivity caused by the oxygen-plasma treatment suggests that the crystallized silicon films had defect states which were electrically active and trapped some electron carriers. The oxygen-plasma treatment reduced the density of the defect states so that the carrier density increased. Figure 8 shows the electrical conductivity as a reciprocal function of the absolute temperature for the phosphorus-doped silicon films crystallized at a 75-V application. As for the crystallized sample, the electrical conductivity increased with an activation energy of 0.15 eV. Oxygen-plasma treatment reduced the activation energy to 0.11 eV.

We analyzed the changes in the electrical conductivity with temperature using a statistical thermodynamic analysis program [12, 19–21]. We introduced deep level defect states at the mid-gap as well as tail states, whose density exponentially decreased toward the deep energy level in the bandgap, at the grain boundaries. Electron carriers are generated from the phosphorus dopant atoms via ionization, and their probabilities are determined using the Fermi–Dirac statistical distribution function. Free carriers are trapped by the localized defect states and the defects are charged negatively. The Fermi energy level is determined using the statistical thermodynamical conditions, keeping charge neutrality among the densities of ionized dopant atoms (N_d), defect states charged negatively with electron carriers (X_d) and free carriers (n), $N_\mathrm{d} = n + X_\mathrm{d}$, in the whole region including the crystalline grains and grain boundaries. The space-charge effect in the crystalline grains causes band bending and results in the potential barrier at the grain boundaries. In this analysis, the grain size was assumed to be 50 nm, which was the lowest size in the TEM observation. Agreement between the temperature dependencies of the calculated and experimen-

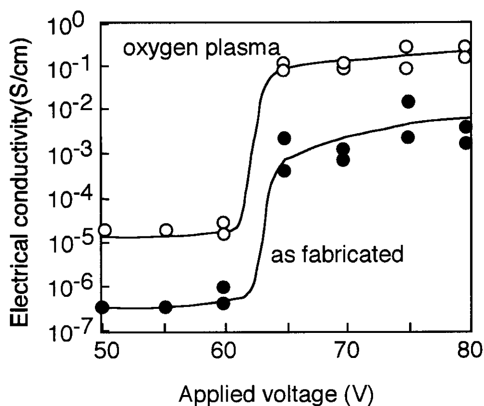

Fig. 7. Electrical conductivity as a function of the voltage applied to the Cr strips for 7×10^{17}-cm^{-3} phosphorus-doped silicon films before (*solid circles*) and after (*open circles*) oxygen plasma treatment at 250 °C and 100 W for 5 min

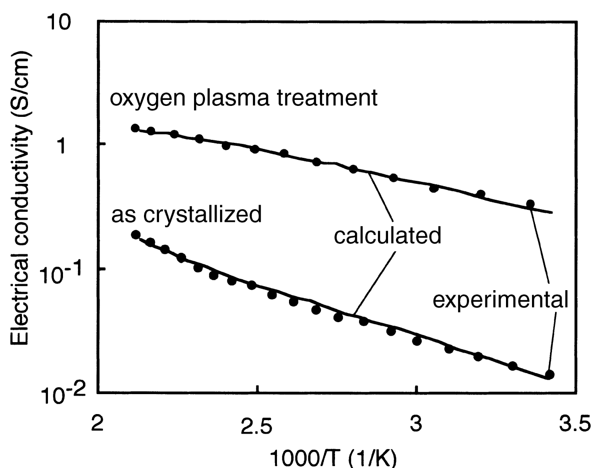

Fig. 8. Electrical conductivity measured (*dots*) and calculated (*solid curves*) as a reciprocal function of the absolute temperature for 7×10^{17} cm^{-3} phosphorus-doped silicon films crystallized at a 75-V application. The electrical conductivity is shown for films before and after oxygen-plasma treatment at 250 °C and 100 W for 5 min

tal conductivities resulted in the densities of the defect states being at a deep level, as well as tail states. The silicon films crystallized at a 75-V application had a density of defect states of $8.0 \times 10^{17}\,\mathrm{cm}^{-3}$ at the mid-gap energy level and tail states of density $1.0 \times 10^{19}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$ at the conduction band edge, and the width, at which the tail state density decreased to e^{-1} of the peak density at the band edge, was 0.15 eV. The potential barrier height at the grain boundaries was 0.19 eV. On the other hand, oxygen-plasma treatment at 250 °C and 100 W for 5 min reduced the density of the defect states at the mid-gap to $2.7 \times 10^{17}\,\mathrm{cm}^{-3}$ and the width of the tail states to 0.13 eV. The potential barrier height consequently decreased to 0.1 eV.

The present crystallization and activation method will be useful for the fabrication of electronic devices such as TFTs. Rapid crystallization of the buried silicon layer shown in Fig. 5 suggests the variety of the crystallization step. Crystallization of silicon films after gate insulators and gate electrodes would be possible. The present method would be also useful for rapid heating of insulating materials and insulator/semiconductor interfaces, reducing defects.

3 Summary

We reported a simple crystallization method for silicon films using electrical-current-induced Joule heating at the Cr strips formed on 50-nm-thick silicon films via 200-nm-thick SiO_2 intermediate layers. 3-μs-pulsed voltages were applied to the Cr strips with a length of 250 μm and a width of 50 μm. The high heating intensity above $1 \times 10^5\,\mathrm{W/cm}^2$ was easily achieved by letting the electrical current flow in the Cr strips. The high Joule heating intensity of about $1 \times 10^6\,\mathrm{W/cm}^2$ occurred due to a reduction in the Cr resistivity because of melting at 90-V application. The Joule heating energy density varied between 0.4 and $2.5\,\mathrm{J/cm}^2$ by changing the voltage from 50 to 90 V. Numerical heat flow analysis suggested that the silicon films were heated to the melting point of silicon using electrical-current-induced Joule heating generated above $1.4\,\mathrm{J/cm}^2$. Heat generated at the Cr strips rapidly diffused to the underlying SiO_2 intermediate layers and heated the silicon films below the SiO_2 layers. Raman scattering measurements revealed that the silicon films were completely crystallized at a Joule heating energy of $1.9\,\mathrm{J/cm}^2$. There was a tensile stress of 1.3×10^9 Pa in the silicon films. Transmission electron microscopy measurements confirmed a crystalline grain size of 50–100 nm. 1-μm-long crystalline grain growth was also observed in the region just beneath the edge of the Cr strips. The large grain growth probably occurred because of the temperature gradient in the lateral direction caused by heat dissipation at the edge of the Cr strips. The electrical conductivity increased from 10^{-6} S/cm to 0.02 S/cm for $7 \times 10^{17}\text{-cm}^3$ phosphorus-doped silicon films because of activation of the phosphorus atoms due to crystallization. Oxygen-plasma treatment at 250 °C and 100 W for 5 min further increased the electrical conductivity to 0.3 S/cm. The statistical thermodynamical analysis of the electrical conductivity gave a density of defect states of $8.0 \times 10^{17}\,\mathrm{cm}^{-3}$ at the mid-gap energy level and tail states whose density was $1.0 \times 10^{19}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$ at the conduction band edge, and the width, at which the tail state density decreased to e^{-1} of the peak density at the band edge, was 0.15 eV. The potential barrier height at the grain boundaries was 0.19 eV. Oxygen-plasma treatment at 250 °C and 100 W for 5 min reduced the density of defect states at the mid-gap to $2.7 \times 10^{17}\,\mathrm{cm}^{-3}$ and the width of the tail states to 0.13 eV. The potential barrier height consequently decreased to 0.1 eV.

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