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Improvement of Gate-Insulator/Silicon Interface Characteristics in Amorphous Silicon Thin Film Transistors

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N-channel Al-top gate type amorphous silicon thin film transistors (a-Si TFTs) were fabricated with an SiO_2 gate oxide, never exceeding a substrate temperature of 250°C. A reactive evaporation of SiO powder in an oxygen atmosphere with a flow rate of 2 sccm at a pressure of 1×10^{-4} Torr was used for forming a good quality interface of SiO_2/a-Si. The a-Si TFTs showed characteristics of a low threshold voltage of 0.86 V, a moderate carrier mobility of 1.1 $cm^2/V\cdot s$ and a subs-threshold slope of 0.12 V/decade. These characteristics result from a good SiO_2/a-Si interface with a density of trapping states of 1.6×10^{11} $cm^{-2}\cdot eV^{-1}$.

KEYWORDS: top gate type a-Si TFF, SiO evaporation, laser crystallization, interface trapping density

Amorphous silicon thin film transistors (a-Si TFTs) have been widely investigated as switching transistors for display elements in liquid crystal display panels.[1-4] The TFTs can be fabricated on a large area and cheap glass substrates because both hydrogenated amorphous silicon (a-Si:H) and silicon nitride (SiN) films are easily fabricated as an active layer and a gate insulator, respectively, at a temperature lower than 350°C using plasma enhanced chemical vapor deposition (PECVD). Bottom-gate type transistors are widely used because serious plasma damage is thereby not caused at the interface of a-Si:H/SiN. On the other hand, It has been difficult to fabricate top-gate-type a-Si TFTs with a threshold voltage below 2 V using PECVD because plasma damage causes large interface trapping sates during formation of gate insulator.[5] Still there remains a clear process advantage with top gate methodology to more easily form the self-aligned gate structure using ion-implantation methods with mass separation[5] or without mass separation,[6,7] which can minimize a stray capacitor.

We have recently demonstrated that a simple method of reactive and thermal evaporation of SiO in an oxygen atmosphere realizes formation of SiO_2 films with a low damage at room temperature because there is no electrons and ions with high energy which can cause defects.[8] Top-gate type poly-Si TFTs fabricated with the SiO_2 had a density of interface trapping states of 1.4×10^{11} cm^{-2}/eV^{-1}.[8]

In this paper, the same method of SiO evaporation is applied to forming a good SiO_2/a-Si interface. And, this paper reports top-gate type a-Si TFTs with a threshold voltage lower than 2 V.

N-channel and top-gate-type a-Si TFTs were fabricated, as shown by a process flow in Fig. 1. First of all, hydrogenated amorphous silicon films doped with 2%-phosphorus with a thickness of 20 nm were formed on glass substrates at 250°C using PECVD. The doped films were removed at the channel region with a length of 10 μm by etching. Undoped a-Si:H films with a thickness of 20 nm were then deposited using PECVD over the whole area. The silicon layers were then patterned by etching for isolation.

A 150 nm-thick SiO_2 layer was subsequently deposited as the gate insulator using the SiO evaporation with an oxygen atmosphere,[8] as shown in Fig. 1. A Ta boat with having a powder of SiO with a purity of 99.99% was connected to the electrodes placed in a vacuum chamber. A sample was placed above the boat. There was a shutter between the boat and the sample. The chamber was evacuated to a pressure lower than 1×10^{-6} Torr. With the shutter closed, a voltage was applied to the Ta boat in order to heat it just below the evaporation threshold for 5 min. After the applied voltage was reduced to 0 V to cool the Ta boat, oxygen gas

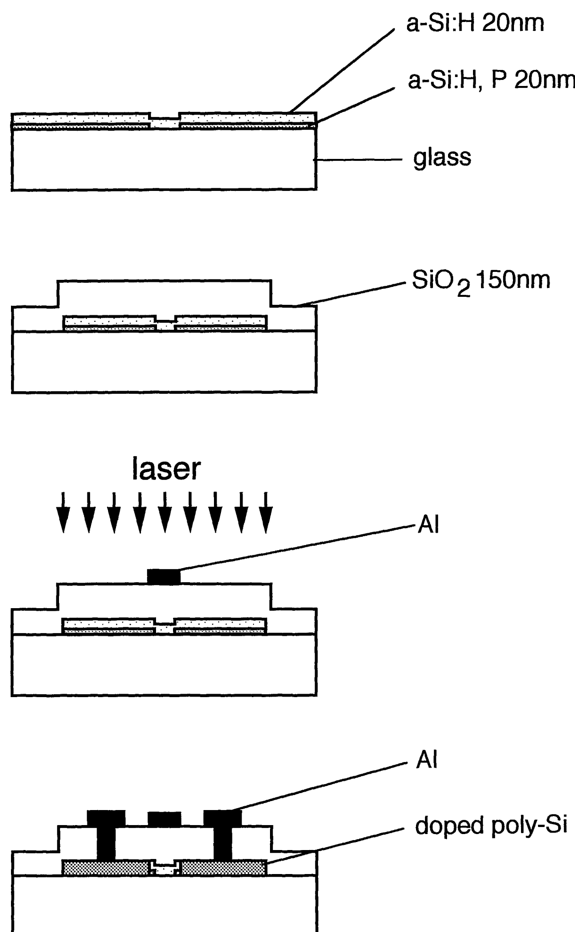

Fig. 1. Cross section of TFT during fabrication.

with the flow rate of 2 sccm was then introduced. The Ta boat was heated again and SiO was evaporated in an oxygen ambient. SiO_2 films were formed on a substrate after the shutter was open. The deposition rate was 10 nm/min. Hot molecular SiO (maybe clusters with some molecules) evaporated from heated SiO powders effectively react with oxygen gas and SiO_2 films are formed on substrates at room temperature. C-V measurements for Al-gate MOS capacitor fabricated in single crystallne Si revealed that a SiO_2/Si interface with an interface trapping density lower than 5×10^{10} $cm^{-2}\cdot eV^{-1}$ is formed by the method of SiO evaporation with a oxygen flow rate of 2 sccm. The break down voltage of the SiO_2 films was about 2 MV/cm.

Al metal layer was evaporated, after the SiO_2 film formation. Al gate electrodes with a length of 14 μm were defined by etching. There was 2 μm overlap between the Al gate and doped a-Si layers at both edges of the channel region. Laser irradiation with 30 ns-pulsed XeCl excimer laser was provided in vacuum at substrate temperature of 250°C in order to form source and drain regions, as can be seen in Fig. 1. The silicon layers were melted and then crystallized by laser irradiation with an energy density of 190 mJ/cm^2 through the SiO_2 layer.[5,9] Phosphorus atoms were diffused into the overlaying silicon layer throughout whole thickness during the laser crystallization. Doped regions with a conductivity of 500 S/cm were formed by irradiation, while phosphorus doped a-Si:H had a low conductivity of 3×10^{-4} S/cm. Al-source and drain electrodes were finally formed by a lift-off method.

Figure 2 shows the output characteristic of the a-Si TFT fabricated with the 150 nm-thick SiO_2 gate insulator formed by the present method. It shows a high drain current with a low gate voltage. Figure 3 shows the drain-current-vs-gate-voltage characteristic of the a-Si TFT. The TFT had a low threshold voltage of 0.86 V with an effective carrier mobility in the linear region of 1.1 cm^2/V·s. The sub-threshold slope was 0.12 V/decade. These characteristics shows that the method of SiO evaporation realized a good SiO_2/Si interface compared with the conventional method of PECVD. The interface trapping density was estimated using the sub-threshold slope when it was assumed that no depletion region is formed in silicon layers because the thickness of the silicon films in the channel region was very thin (20 nm).[10] The sub-threshold slope (S) was described as following equation,

$$S=kT/q\times\ln 10\times(1+eD_{it}/C_{ox}) \quad (1)$$

where k is the Boltzman constant, T is the absolute temperature, e is the electron charge, D_{it} is the interface trapping density, C_{ox} is the capacitance of SiO_2. In the eq. (1), there is no component of capacitance caused by a depletion region in contrast to field effect transistors fabricated in silicon substrates. From the eq. (1) and experimental results of the sub-threshold slope, the defect density was estimated to be 1.6×10^{11} $cm^{-2}\cdot eV^{-1}$.

These results suggest that there will be a possibility to apply top-gate type a-Si TFTs with good characteristics to electronic devices which require a high switching speed such as switching elements for high definition television.

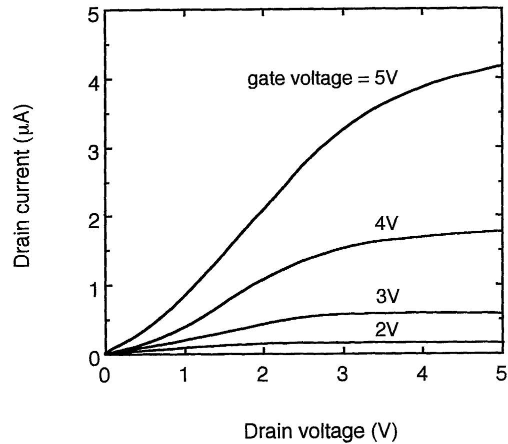

Fig. 2. Drain current vs drain voltage characteristics of the a-Si TFT. The gate length and gate width are 10 μm and 80 μm, respectively.

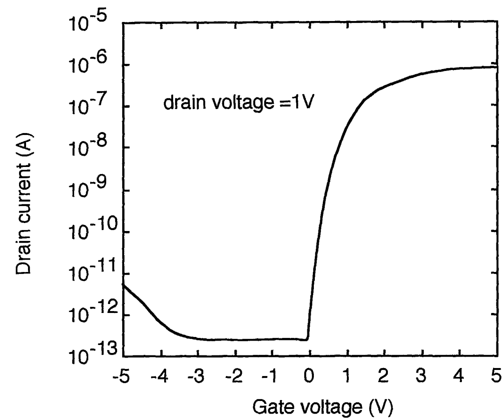

Fig. 3. Drain current vs gate voltage characteristics of n-channel and p-channel poly-Si TFTs with the 150 nm-thick SiO_2 gate insulator fabricated by the present method. Drain voltage is 1 V. The gate length and gate width are 10 μm and 80 μm, respectively.

In summary, reactive and thermal evaporation of SiO in an oxygen atmosphere was applied to forming a good SiO_2/Si interface in a-Si TFFs at room temperature. N-channel and Al-top-gate a-Si TFTs were fabricated at 250°C with the present SiO_2 gate oxide films and laser heating for forming source and drain regions using a 30 ns-pulsed XeCl excimer laser. The TFTs showed a low threshold voltage of 0.86 V and a carrier mobility of 1.1 cm^2/V·s. The interface defect density was 1.6×10^{11} $cm^{-2}\cdot eV^{-1}$. These characteristics result from the fact of that SiO_2 films are formed on the amorphous silicon surface with low damage.

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1) P. G. LeComber, W. E. Spear and A. Gaith: Electronic Lett. **15** (1979) 179.

2) Y. Kaneko, A. Sasano and T. Tsukada: IEEE Trans. Electron Devices **ED-36** (1989) 2953.
3) K. Suzuki: *Proc. Amorphous & Microcrystalline Semiconductor Devices*, ed. J. Kanicki (Artech Hoise, Boston, 1991) p. 77.
4) B. C. Ahn, K. Shimizu, T. Satoh, H. Kanoh, O. Sigiura and M. Matumura: Jpn. J. Appl. Phys. **30** (1991) 3625.
5) T. Sameshima, S. Usui and M. Sekiya IEEE Electron Device Lett. **EDL-7** (1986) 276.
6) G. Kawachi, T. Aoyama, T. Suzuki, A. Mimura, Y. Ohno, N. Konishi and Y. Mochizuki: Ext. Abstr. 22nd Conf. Solid State Devices & Materials, Sendai, 1990, p. 971.
7) K. Masumo, M. Kunigita, S. Takafuji, N. Nakamura, A. Iwasaki and M. Yuki: Ext. Abstr. 22nd Conf. Solid State Devices & Materials, Sendai, 1990, p. 975.
8) T. Sameshima, A. Kohno, M. Sekiya, M. Hara and N. Sano: Appl. Phys. Lett. **64** (1994) 1018.
9) T. Sameshima, M. Hara and S. Usui: Proc. Mater. Res. Soc. Symp. **158** (1990) 255.
10) S. M. Sze: *Physics of Semiconductor Devices* (John Wiley & Sons, New York, 1981) 2nd ed., Chap. 8.