XeCl Excimer Laser Annealing Used in the Fabrication of Poly-Si TFT's

T. SAMESHIMA, S. USUI, AND M. SEKIYA

Abstract—**Mo-gate n-channel poly-Si thin-film transistors (TFT's) have been fabricated for the first time at a low processing temperature of 260°C. A 500–1000-A-thick a-Si:H was successfully crystallized by XeCl excimer laser (308 nm) annealing without heating a glass substrate. TFT's were fabricated in the crystallized Si film. The channel mobility of the TFT was 180 cm²/V·s when the a-Si:H was crystallized by annealing with a laser having an energy density of 200 mJ/cm². This result shows that high-speed silicon devices can be fabricated at a low temperature using XeCl excimer laser annealing.**

I. Introduction

A TECHNIQUE for the fabrication of thin-film transistors (TFT's) at low temperature is very useful for devices such as a liquid crystal display matrix. For this reason, a-Si TFT's which can be fabricated at a processing temperature of 200–300°C have been widely used [1], [2]. However, a-Si TFT's have a channel mobility of no more than 1 cm²/V·s. Therefore they cannot be applied to devices, such as a shift register, which operate at a high speed. On the other hand, poly-Si TFT's are more suitable for devices which operate at a high speed [3]–[5], because they can have a much higher channel mobility than a-Si TFT's. However, to fabricate poly-Si TFT's using conventional processes, the temperature must be very high (600–1000°C).

In this paper, we present for the first time a new technique for fabricating poly-Si TFT's at 260°C using XeCl excimer laser annealing. To fabricate a poly-Si film at low temperature, an a-Si:H film deposited on a glass substrate was crystallized by annealing with a XeCl excimer laser (308 nm). Since the absorption coefficient of the a-Si:H is 1×10^6 cm^{-1} at 308 nm [6], the laser pulse was absorbed up to 200 A below the surface of the film. During a laser pulsewidth of 35 ns, only the top 1000-A layer from the surface was heated to a high temperature. When annealed, therefore, the a-Si:H thin film was crystallized without heating the substrate. TFT's were then fabricated in the crystallized Si film on a glass substrate at a processing temperature of 260°C.

II. Experiment

Mo-gate n-channel poly-Si TFT's were fabricated on a TEMPAX glass substrate by the process using the XeCl excimer laser annealing as shown in Fig. 1.

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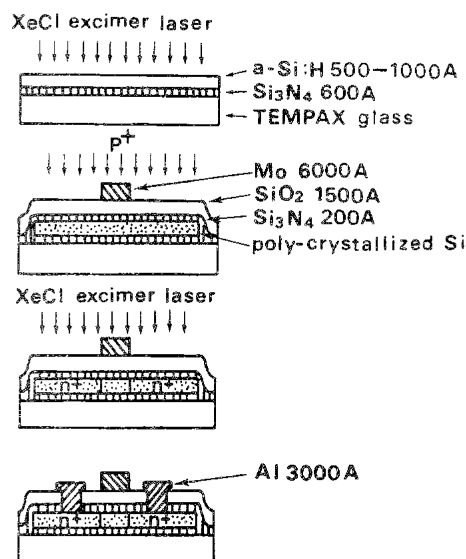

Fig. 1. Schematic cross section of the poly-Si TFT during the fabrication process.

Using plasma CVD, a 600-A-thick silicon nitride (Si_3N_4) layer and a 500–1000-A-thick a-Si:H layer were successively deposited on the substrate at 260°C. Then, the a-Si:H layer was crystallized at room temperature during the XeCl excimer laser annealing. Fig. 2 shows the schematic diagram of the apparatus used for laser annealing. The sample was placed perpendicular to a laser beam in a vacuum chamber as can be seen in the figure. The substrate was not heated. A pulsed excimer laser at a rate of 10 pps was focused on and scanned across the surface of the sample at a speed of 1–5 mm/s using an optical scanning device mounted on an X–Y stage. There was no deformation of the glass substrate during laser treatment. TEM observation of the crystallized film revealed that grain size grew to be 1000 A after being annealed by a laser with an energy density about 200 mJ/cm². Furthermore, IR absorption measurement revealed that the 1000-A grain polysilicon still contained about 1-atomic percent of hydrogen atoms at grain boundaries. The hydrogen atoms efficiently terminated dangling bonds of poly-Si and reduced barrier height of grain boundaries. Therefore we believe that the poly-Si can have a large mobility. After the crystallization, the poly-Si and Si_3N_4 island was defined by etching. Next, using plasma CVD, 200-A-thick Si_3N_4 and 1500-A-thick SiO_2 layers were deposited as gate insulators at 260°C. A 6000-A-thick Mo layer was subsequently deposited by sputtering. The gate electrode was defined by etching. The source and drain regions were formed by 130-keV P^+ ion implantation at a dose

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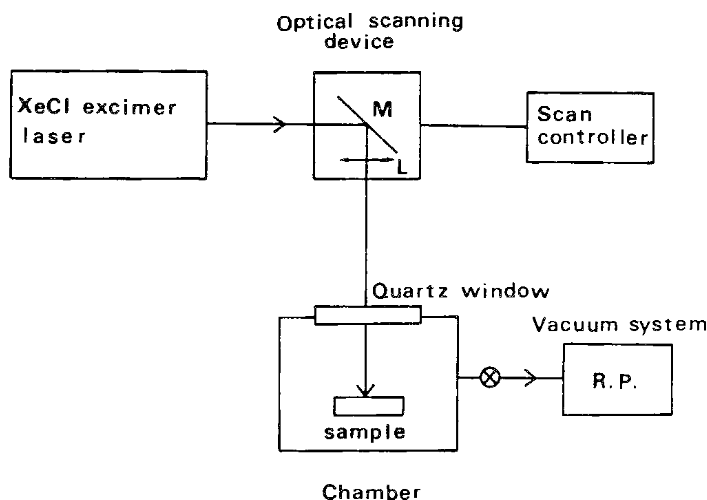

Fig. 2. Schematic diagram of the apparatus for XeCl excimer laser annealing.

of 2×10^{15} cm^{-2}. Activation of implanted phosphorous was carried out at room temperature using XeCl excimer laser annealing. Conductivity of the n^+ region was 100 S·cm^{-1}. SIMS measurement revealed that an in-depth profile of the dopant concentration did not change during laser annealing. Therefore there was no redistribution of dopants. After contacts were opened, a 3000-Å-thick Al layer was evaporated and the source and drain electrodes were defined by etching.

III. Results

TFT's measuring $W(160\ \mu m)/L(20\ \mu m)$ were fabricated. To evaluate the TFT's characteristics, I_D–V_D and I_D–V_G characteristics were measured. The channel mobility was determined by measuring the saturation current. Figs. 3 and 4 show the I_D–V_D and I_D–V_G characteristics. The poly-Si TFT was fabricated using the following laser annealing condition: 70 laser pulses with an energy density of 200 mJ/cm^2 were applied to cause crystallization, and 100 laser pulses with an energy density of 180 mJ/cm^2 were applied to cause activation. In Fig. 4, the I_D–V_G characteristic of the poly-Si TFT is compared with that of the a-Si TFT fabricated using the steps described in Fig. 1 excluding the crystallization process by laser annealing. The poly-Si TFT's saturation drain current was much larger than that of the a-Si TFT. The channel mobilities were 152 cm^2/V·s for the poly-Si TFT and 0.3 cm^2/V·s for the a-Si TFT. The channel mobility increased as the laser energy density for crystallization increased from 150 to 200 mJ/cm^2. TFT's maximum channel mobility was 180 cm^2/V·s as a-Si:H was crystallized by annealing with a laser having an energy density of 200 mJ/cm^2. This probably resulted from the increased grain size in the channel region during crystallization and dangling bonds termination by hydrogen atoms at grain boundaries. Threshold gate voltage of the TFT's was 3 V. However, the drain leakage current value (at $V_G \leq 0$ V) of the poly-Si TFT's also exceeded that of the a-Si TFT as shown in Fig. 4. This results from the fact that no channel doping (B^+ doping) was conducted. Moreover, many defects were probably produced during laser annealing, so that i-n^+ junctions were not perfectly formed. Therefore we think this made the leakage current still larger. However, we have found that a leakage current can be reduced by a subsequent furnace annealing (260°C) after laser annealing.

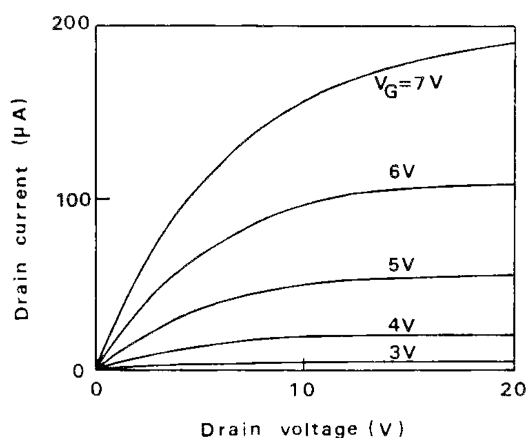

Fig. 3. Drain current versus drain voltage characteristics of the poly-Si TFT measuring $W(160\ \mu m)/L(20\ \mu m)$.

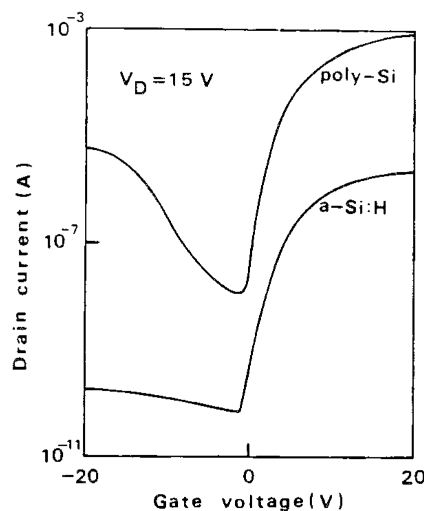

Fig. 4. Drain current versus gate voltage characteristics of the poly-Si TFT and of the a-Si:H TFT fabricated using the steps described in Fig. 1 excluding the crystallization process by laser annealing.

IV. Conclusion

The crystallization of a-Si:H deposited on a glass substrate was successfully carried out at room temperature using the

XeCl excimer laser annealing. TFT's fabricated in a crystallized film at a processing temperature of 260°C had a maximum channel mobility of 180 $cm^2/V \cdot s$. This result shows that high-speed Si devices can be fabricated at a low processing temperature. Therefore we conclude that the XeCl excimer laser annealing process will make low-temperature fabrication of silicon devices possible.

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References

[1] A. J. Snell, K. D. Mackenzie, W. E. Spear, and P. G. LeComber, *Appl. Phys.*, vol. 24, p. 357, 1981.

[2] Y. Ugai, Y. Murakami, J. Tamamura, and S. Aoki, in *SID Symp. Dig.*, 1984, p. 308.

[3] Y. Oana, H. Kotake, N. Mukai, and K. Ide, in *Proc. 14th Conf. Solid State Devices* (Tokyo, Japan), 1982; also *Japan. J. Appl. Phys.*, vol. 22, Suppl. 22-1, p. 493, 1982.

[4] M. Matsui, J. Owada, Y. Shiraki, E. Maruyama, and H. Kawakami, in *Proc. 14th Conf. Solid State Devices* (Tokyo, Japan), 1982; also *Japan. J. Appl. Phys.*, vol. 22, Suppl. 22-1, p. 497, 1982.

[5] S. Morozumi, K. Oguchi, S. Yazawa, T. Kodaira, H. Oshima, and T. Mano, in *SID Symp. Dig.*, 1983, p. 156.

[6] G. D. Cody, C. R. Wronsky, B. Abeles, R. B. Stephens, and B. Brooks, *Solar Cells*, vol. 2, p. 227, 1980.